33. (Twice Amended) A method for accessing a storage device, comprising:
receiving a first address to the storage device;
selecting between [a] an asynchronously-accessible burst mode and [a] an asynchronously-accessible pipelined mode of operation of the storage device;
selecting between outputting information from the storage device and inputting information to the storage device;
obtaining a second address to the storage device; and
asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address[; and]. → ? Burst or Pipeline
[the storage device being asynchronously-accessible in either of the burst mode and the pipelined mode.]

50. (Twice Amended) A system comprising:
a microprocessor;
a memory coupled to the microprocessor, [for operating] the memory in selectively operable either in a burst mode or a pipelined [modes] mode, wherein the memory is an asynchronous dynamic random access memory; and
a system clock coupled to the microprocessor.--

REMARKS

Claims 1, 33 and 50 have been amended. Claims 1-9, 33-35, 46, and 48-50 are presently pending before the Examiner. Further examination and reconsideration are respectfully requested in view of the remarks made in this Response.

The undersigned is not aware of any change in status of the related U.S. patent application(s) or patent(s).

Claims 1-9, 33-35, 46, and 48-50 were rejected under U.S.C. § 102(b) as being anticipated by Manning (U.S. Pat. No. 5,610,864). Specifically, with respect to independent Claims 1, 33, 46 and 50 (all the presently pending independent claims), the Examiner states in relevant part:

> "As to claims 1, 33, and 46, *Manning* discloses the invention as claimed. *Manning* discloses an asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16) capable to switch between pipelined mode (col. 5 lines 43-50) and burst mode (col. 6 lines 14-16); and piplined/burst circuitry coupled to the modem selection circuitry and configured to select between two modes. (Fig. 1 and Ref. 40 and col. 6 lines 14-16)."; and
>
> "As to claim 50, Manning further discloses a microprocessor (Fig. 11 Ref. 112). It is inherent that there is a system clock in the microprocessor to operate the processor."

Applicants agree with the Examiner with respect to an EDO memory constituting an asynchronous memory and a microprocessor having a system clock. However, it is Applicants' position that Manning does not describe, show or suggest an asynchronously-accessible storage

device capable of switching between operating in a pipelined mode and a burst mode. Accordingly, Applicants traverse the Examiner's rejection of Claims 1-9, 33-35, 46 and 48-50.

Manning describes a burst read cycle for an EDO DRAM (col. 4, lines 29-55). Addresses are advanced with one or more pulses of a column-address-strobe signal ("/CAS") (col. 4, line 56, to col. 5, line 8). Next, Manning describes a prefetch architecture for a SDRAM (col. 5, lines 9-42). Accordingly, in the following paragraph, where Manning states that "[o]ther memory architectures...include a pipelined architecture..." (col. 5, lines 43-50), Manning is referring to a synchronous device, such as an SDRAM. Thus, Manning suggests that his burst architecture may be used in an SDRAM with a prefetch architecture and/or a pipelined architecture.

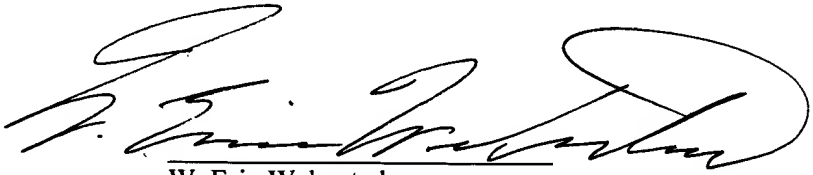
In contrast to the Examiner's contention, it is Applicants' position that Manning does not describe, show or suggest an asynchronously-accessible storage device switchable between a burst mode and a pipelined mode. By way of example, Claim 1 recites:

> An asynchronously-accessible storage device comprising:
>
> mode circuitry configured to select between a burst mode and a pipelined mode; and
>
> circuitry operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.

Notably, Claim 1 includes pipelined/burst circuitry configured to switch between a pipelined mode and a burst mode for operating an asynchronously-accessible storage device. Claims 33, 46, and 50 each recite a same or similar limitation to that of Claim 1. Accordingly, it is respectfully submitted that Claims 1, 33, 46 and 50, all the pending independent claims, are not described, shown or suggested by Manning. Claims 2-9, 34-35 and 48-49 all depend on an allowable claim, and thus are likewise allowable.

It is submitted that all pending claims are in condition for allowance. Accordingly, such allowance is earnestly solicited.

Respectfully submitted,



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